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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2638	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,160	LI ET AL.	
	Examiner	Art Unit	
	Jason M. Perilla	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15-27,29-35 and 37-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *46-56* is/are allowed.

6)☒ Claim(s) *1-13,15-19,23-25,27,31-35,37,38,40,42,44,45 and 57* is/are rejected.

7)☒ Claim(s) *20-22,26,29,30,39,41,43 and 58* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13, 15-27, 29-35, and 37-58 are pending in the instant application.

Response to Arguments/Amendments

2. In view of the amendments to the claims and arguments filed July 21, 2005, the claim objections, rejections under 35 U.S.C. § 112, first and second paragraphs, and prior art rejections under 35 U.S.C. §103(a) filed in the first office action dated March 28, 2005 have been withdrawn.

3. New objections and prior art rejections are set forth below.

Claim Objections

4. Claims 9, 24-27, 29, and 37-41 are objected to because of the following informalities:

Regarding claim 9, in line 2, "of each of" should be replaced by –of each--.

Regarding claim 24, in line 2, "the second plurality of latching circuits" is lacking antecedent basis.

Regarding claim 25, the claim is objected to for the same reasons as applied to claim 24 above.

Regarding claim 26, the claim is objected to for the same reasons as applied to claim 24 above.

Regarding claim 27, the claim is objected to for the same reasons as applied to claim 24 above.

Regarding claim 29, the claim is objected to for the same reasons as applied to claim 24 above.

Regarding claims 37-40, the claims are objected because they depend upon claim 36 which is cancelled.

Regarding claim 41, in lines 1-2, "the reference clock" is lacking antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 6-12, 16-19, 23-25, 27, and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubinec (US 5900834 – previously cited).

Regarding claim 1, Kubinec discloses a circuit for jitter measurement according to figure 3(a), comprising: a plurality of delay elements (plurality of delay elements 302(a) and 302(b)) arranged in a series-connected chain having a total delay equal to the sum of the delays of the delay elements, wherein the first element in the chain has an input that receives an input clock signal (DLYIN), the chain propagating the input clock signal through each of its elements, and each delay element output producing a delayed version of the signal on its input; a first set of circuitry (304) operative to produce at an output a pulse corresponding to each delay element (each delay element 302(a) and 302(b)) in response to the propagation of a significant instant or edge (col. 6, lines 33-39) of the input clock signal through the delay elements each pulse having a

width that is approximately equal to the delay of the corresponding delay element; and a second set of circuitry (305) having one storage element corresponding to each output of he first set of circuitry, and an input (MASTER CLOCK) that receives a trigger signal, that is timed to correspond to a delay which is approximately half of the total delay of the chain, and the second set of circuitry being operative to record in the corresponding storage element (col. 2, lines 9-13; col. 3, lines 59-61) any pulse that is active at the time of occurrence of the trigger signal, wherein a jitter measurement is made based on the pulses recorded in the storage elements after a plurality of trigger signals or mean has occurred (col. 2, lines 9-13; col. 3, lines 59-61; col. 4, lines 15-20). The total delay is equal to the sum of the delays of the individual delay elements because the delay elements are serially connected as illustrated in figure 3(a). The output of one delay element is input to the next delay element such that the total delay is additive. The pulses corresponding to each delay element which are generated by the first set of circuitry have a width that is approximately equal to the delay of its corresponding delay element because, as illustrated in figure 3(a), each pulse's width is determined according to the difference between the input and the output of its delay stage. Therefore, it can only be as wide as its corresponding delay allows. Kubinec does not explicitly disclose that the trigger signal (fig. 3(a), MASTER CLOCK) is timed to correspond to a delay which is approximately half of the total delay of the chain. However, the correct choice of the trigger signal timing is imperative for the utility of the circuit. That is, if the trigger timing is chosen improperly, the significant instant of the input clock signal may be lost. It is implied by Kubinec or at least obvious to one having

ordinary skill in the art that the delay line is chosen to be of the appropriate length to capture the significant instant of the input clock signal as close to the middle of the delay line as possible so that it would be captured regardless of occurring early or late. That is, the best chances for capturing the significant instant of the input clock signal is to trigger the delay line according to the mid point of its delay..

Regarding claim 2, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec discloses that the output of one delay element is connected to the input of the next adjacent delay element (fig. 3(a)).

Regarding claim 3, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec discloses that the number of delay elements in the chain is N, where N is a number greater than 2 (fig. 3(a); col. 6, lines 25-40). Kubinec does not explicitly disclose that the delay line is implemented as a power of 2. However, it is obvious that the delay line would perform equally well if it had an even or odd number of delay elements. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to implement the delay line as a power of 2. Applicant has not disclosed that implementing the delay line as a power of 2 provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with a delay line implemented as a power of 1 or 2 because the number of delay elements does not need to be an even number for utility of the delay line.Regarding claim 4, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec discloses that the associated delay of each element is controlled by a calibration signal

(figs. 3(b) and 3(c); col. 7, lines 9-20). The calibration signal controls the length of each delay element as illustrated and described. Further, it is inherent that the calibration signal is generated by circuitry or calibration circuitry. Therefore, Kubinec discloses calibration circuitry or a delay control circuit.

Regarding claim 6, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec discloses that the first set of circuitry comprises a plurality of two input logic gates, each two input logic gate corresponding to a respective delay element (fig. 3(a) and figs 4(a-e)).

Regarding claim 7, Kubinec discloses the limitations of claim 6 as applied above. Further, Kubinec discloses that the inputs of the plurality of two-input logic gates are coupled to the input and the output of a corresponding one of the plurality of delay elements (fig. 3(a)).

Regarding claim 8, Kubinec discloses the limitations of claim 7 as applied above. Further, Kubinec discloses that, in various embodiments, one of the two inputs of each two input logic gate is coupled to the output of its corresponding delay element via an inverting logic gate (fig. 5a).

Regarding claim 9, Kubinec discloses the limitations of claim 7 as applied above. Further, Kubinec discloses that one of the two inputs of each two input logic gate is coupled to the output of its corresponding delay element by means of a wired connection (fig. 3(a)).

Regarding claim 10, Kubinec discloses the limitations of claim 6 as applied above. Further, Kubinec discloses that each of the plurality of two input logic gates is

capable of producing a pulse with a width approximately equal to the delay of its corresponding delay element. The pulses corresponding to each delay element which are generated by the first set of circuitry have a width that is approximately equal to the delay of its corresponding delay element because, as illustrated in figure 3(a), each pulse's width is determined according to the difference between the input and the output of its delay stage.

Regarding claim 11, Kubinec discloses the limitations of claim 1 as applied above. Further Kubinec discloses that the second set of circuitry includes a first plurality of latching circuits (fig. 3(a), refs. 306) each corresponding to one of the plurality of delay elements. In figure 3(a), one of the plurality of delay elements consists of the stages 302(a) and 302(b).

Regarding claim 12, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec disclose that the input clock signal (fig. 2(a), "RECEIVE") is related to a reference clock signal (fig. 2(a), "TRANSMIT"). The input clock signal is related to the reference clock signal because the input clock signal is a reflected version of the reference clock signal.

Regarding claim 16, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec discloses that the measure for jitter is filtered or averaged (fig. 2(b), col. 4, lines 15-20).

Regarding claim 17, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec discloses that the second set of circuitry further includes a single one detector for filtering the measure of jitter. The second set of circuitry (fig.

3(a), ref. 306) is a single one detector because it counts a *single* significant instance or single "one" during each triggering master clock (col. 2, lines 9-13; col. 3, lines 59-61; col. 4, lines 15-20).

Regarding claim 18, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec discloses that pulses are recorded for a first number of significant instants of the trigger signal (col. 2, lines 9-13; col. 3, lines 59-61; col. 4, lines 15-20).

Regarding claim 19, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec discloses a third set of circuitry (fig. 2(a), ref. 130) for recording pulses or, as broadly as claimed, a doppler shift.

Regarding claim 23, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec discloses a result calculator configured to provide information collected from the measure of jitter (fig. 2(a), ref. 130).

Regarding claim 24, Kubinec discloses the limitations of claim 19 as applied above. Further, Kubinec discloses a result calculator (fig. 2(a), ref. 130) configured to receive recorded pulses and based thereon providing information on an earliest occurrence in the chain of the significant instant of the propagating input clock signal (fig. 2(b)). Figure 2(b) illustrates the information on the earliest occurrence in the chain of the significant instant each designated by an "X".

Regarding claim 25, Kubinec discloses the limitations of claim 19 as applied above. Further, Kubinec discloses a result calculator (fig. 2(a), ref. 130) configured to receive recorded pulses and based thereon providing information on an latest

occurrence in the chain of the significant instant of the propagating input clock signal (fig. 2(b)). Figure 2(b) illustrates the information on the latest occurrence in the chain of the significant instant each designated by an "X".

Regarding claim 27, Kubinec discloses the limitations of claim 19 as applied above. Further, Kubinec discloses a result calculator (fig. 2(a), ref. 130) configured to receive recorded pulses and based thereon providing median or average information on the occurrences of the significant instant of the propagating input clock signal (fig. 2(b)). Figure 2(b) illustrates the information on the average occurrence in the chain of the significant instant each designated by an "X" (col. 4, lines 15-20).

Regarding claim 57, Kubinec discloses the limitations of the claim as applied to claim 1 above.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kubinec in view of Yoon et al (US 6304116; hereafter "Yoon" – previously cited).

Regarding claim 5, Kubinec discloses the limitations of claim 4 as applied above. Kubinec discloses that the plurality of delay elements have an adjustable delay for properly capturing the significant instant of the input signal (figure 3(c)). Kubinec does not explicitly disclose that the delay control circuit is a charge pump controlled delay lock loop. However, Yoon teaches by figure 4 an exemplary plurality of delay elements (d1-dn) wherein the delay of each individual element is varied according to a voltage (VCON) determined by a charge pump (ref. 45; col. 3, lines 10-23). One skilled in the art is familiar with voltage controlled delay lines and the benefit of accuracy they provide. Therefore, it would have been obvious to one having ordinary skill in the art at

the time which the invention was made to utilize a charge pump controlled delay line as taught by Yoon in place of the plurality of delay elements of Kubinec because the individual delays of each of the delay elements could be more accurately chosen for the proper capture of the significant instant of the input signal.

8. Claims 13, 15, 31-35, 37, 38, 40, 42, 44, 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubinec in view of Riedle et al (US 6795515; hereafter "Riedle" – previously cited).

Regarding claim 13, Kubinec discloses the limitations of claim 12 as applied above. Further, according to figure 2(a) of Kubinec, as understood by one having skill in the art, the reference generator oscillator (200) produces the trigger signal "MASTER CLOCK" of figure 3(a) used to latch the output of the edge detectors into memory. The phase or jitter difference is measured between the latched edge of period detection logic (220) against the latched edge of period detection logic (222) by the Doppler shift detector (230). Kubinec does not explicitly disclose that the trigger signal is delayed from the reference clock signal by a second delay. However, Riedle teaches a method of capturing a significant instant of a signal. Figure 2 of Riedle illustrates an input "DATA IN" which is fed into a delay line 24 and latched into latches 26. Further, Riedle teaches that the input signal must be accurately sampled or latched at the correct time to capture the significant instant of the input signal (col. 3, lines 20-62). The processor (fig. 2, ref. 25) applies a programmable delay to the clock signal (4ns o_CLOCK) such that the latches capture the significant instant of the delay line. One skilled in the art would readily apply the teachings of Riedle to the method of Kubinec because the

timing of the trigger signal should be such that the latches of both the detection logics (fig. 2(a), refs. 220 and 222) are latched at a time when the difference in significant instants may be compared. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a programmable delay on the trigger signal of Kubinec to create the delayed trigger signal as taught by Riedle because the appropriate timing of the trigger signal is needed to measure the jitter between the transmit and receive signals.

Regarding claim 15, Kubinec in view of Riedle disclose the limitations of claim 13 as applied above. Further, in the circuit of Kubinec in view of Riedle, it would be necessary to compare the latched significant instant to the first predetermined delay to determine a measure for jitter because the first predetermined delay determines, in part, the timing of the latched significant instant. That is, the jitter measurement can only be made by using both the information from the latched significant instant on the delay line and the timing of the first significant instant.

Regarding claim 31, Kubinec discloses a method for measuring jitter of a clock signal, comprising: for each of a plurality of trigger signal occurrences (col. 2, lines 25-35), performing the steps of; receiving the clock signal (fig. 3(a), "DLYIN"), the clock signal having a significant instant or edge (col. 6, lines 33-39); propagating the significant instant of the clock signal through a chain of delay elements (fig. 3(a), ref. 302), wherein each element as an associated delay and the chain has a total delay equal to the sum of the associated delays; receiving a trigger signal (fig. 3(a), "MASTER CLOCK"); detecting propagation of the significant instant of the clock signal

through each of the delay elements in the chain and producing a pulse corresponding thereto (fig. 3(a), ref. 304); recording any pulse that is coincident with the trigger signal (fig. 3(a), ref. 306); and producing a jitter measurement signal (fig. 2(a), output of period detection logic 220) responsive to the recorded pulses after the plurality of trigger signal occurrences. Kubinec does not explicitly discloses delaying the trigger signal to occur at a time equal to approximately half the total delay of the chain. However, Riedle teaches a method of capturing a significant instant of a signal. Figure 2 of Riedle illustrates an input "DATA IN" which is fed into a delay line 24 and latched into latches 26. Further, Riedle teaches that the input signal must be accurately sampled or latched at the correct time to capture the significant instant of the input signal (col. 3, lines 20-62). The processor (fig. 2, ref. 25) applies a programmable delay to the clock signal (4ns o_CLOCK) such that the latches capture the significant instant of the delay line. One skilled in the art would readily apply the teachings of Riedle to the method of Kubinec because the timing of the trigger signal should be such that the latches of both the detection logics (fig. 2(a), refs. 220 and 222) are latched at a time when the difference in significant instants may be compared. Further, as applied to claim 1 above, it is implied by Kubinec or at least obvious to one having ordinary skill in the art that the delay line and the delay of the trigger signal is chosen to be of the appropriate time length to capture the significant instant of the input clock signal as close to the middle of the delay line as possible so that it would be captured regardless of occurring early or late. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a programmable delay on the

trigger signal of Kubinec to create the delayed trigger signal as taught by Riedle because the appropriate timing of the trigger signal is needed to measure the jitter between the transmit and receive signals.

Regarding claim 32, Kubinec in view of Riedle disclose the limitations of claim 31 as applied above. Further, Kubinec discloses deriving a jitter measure (fig. 2(a), "OUT") through the comparison of the jitter measurement signal to an associated delay (fig. 2(a), output of period detection logic 222).

Regarding claim 33, Kubinec in view of Riedle disclose the limitations of claim 31 as applied above. Further, Kubinec discloses that the measure for jitter is filtered or averaged (fig. 2(b), col. 4, lines 15-20).

Regarding claim 34, Kubinec in view of Riedle disclose the limitations of claim 33 as applied above. Further, Kubinec discloses a result calculator (fig. 2(a), ref. 130) configured to receive the filtered jitter measurement signal and based thereon providing information on an earliest occurrence in the chain of the significant instant of the propagating input clock signal (fig. 2(b)). Figure 2(b) illustrates the information on the earliest occurrence in the chain of the significant instant each designated by an "X".

Regarding claim 35, Kubinec in view of Riedle disclose the limitations of claim 33 as applied above. Further, Kubinec discloses a result calculator (fig. 2(a), ref. 130) configured to receive the filtered jitter measurement signal and based thereon providing information on an latest occurrence in the chain of the significant instant of the propagating input clock signal (fig. 2(b)). Figure 2(b) illustrates the information on the latest occurrence in the chain of the significant instant each designated by an "X".

Regarding claim 37, Kubinec in view of Riedle disclose the limitations of claim 31 as applied above. Further, Kubinec discloses the remaining limitations of the claim as applied to claim 33 above.

Regarding claim 38, Kubinec in view of Riedle disclose the limitations of claim 32 as applied above. Further, Kubinec discloses the remaining limitations of the claim as applied to claim 33 above.

Regarding claim 40, Kubinec in view of Riedle disclose the limitations of claim 31 as applied above. Further, Kubinec discloses determining statistical information or an average (fig. 2(b), col. 4, lines 15-20) on the occurrence in the chain of the propagating significant instant.

Regarding claim 42, Kubinec in view of Riedle disclose the limitations of claim 31 as applied above. Further, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to adjust the trigger delay in response to the jitter measurement signal because the jitter measurement signal may determine that more or less delay to the trigger signal is required to properly capture the jitter.

Regarding claim 44, Kubinec in view of Riedle disclose the limitations of claim 31 as applied above. Further, Kubinec discloses that the reference clock signal is input to a circuit or "transmitted and received" to produce the input clock signal (fig. 2(a), "TRANSMIT", "RECEIVE").

Regarding claim 45, Kubinec in view of Riedle disclose the limitations of claim 44 as applied above. Further, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to adjust the trigger delay in response

to the jitter measurement signal because the jitter measurement signal may determine that more or less delay to the trigger signal is required to properly capture the jitter.

Allowable Subject Matter

9. Claims 20-22, 26, 29, 30, 39, 41, 43, and 58 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The indication of allowable subject matter is made regarding claims 46-56.

11. The following is a statement of reasons for the indication of allowable subject matter:

The indication of allowable subject matter is made regarding claims 46-56 because the prior art of record does not disclose a system for responding to jitter comprising a jitter measurement apparatus or method wherein a delay line is used to capture an input signal edge for the measurement of the jitter and further utilizing the jitter measurement to adjust a parameter of the system adaptively.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST. The Applicant is requested to contact the Examiner regarding any of the grounds for rejection set forth above and to discuss any allowable subject matter in the case before responding to this office action.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
November 1, 2005

jmp

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER